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Self-Induced Gate Dielectric for Graphene Field-Effect Transistor

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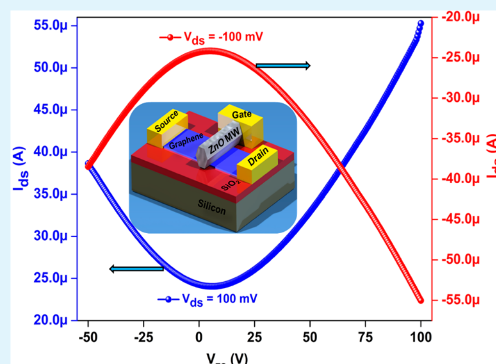
Supporting Information

ABSTRACT: We report the electronic characteristics of an avant-garde graphene-field-effect transistor (G-FETs) based on ZnO microwire as top-gate electrode with self-induced dielectric layer. Surface-adsorbed oxygen is wrapped up the ZnO microwire to provide high electrostatic gate-channel capacitance. This nonconventional device structure yields an on-current of 175 μA, on/off current ratio of 55, and a device mobility exceeding 1630 $cm^2/(V\ s)$ for holes and 1240 $cm^2/(V\ s)$ for electrons at room temperature. Self-induced gate dielectric process prevents G-FETs from impurity doping and defect formation in graphene lattice and facilitates the lithographic process. Performance degradation of G-FETs can be overcome by this avant-garde device structure.



KEYWORDS: *graphene, field effect transistors, ZnO microwire, self-induced, surface oxygen*

A single paper of graphite ignites a revolution in electronics[1] because of its two-dimensional structure and a linear energy dispersion relation, leading to potential application in nanoscale devices.[2] Graphene-based field-effect devices play an immense role in exploring the electronic properties of graphene.[3] Different gate architectures (back, top, and side gate) of graphene field-effect transistors (G-FETs) have their own merits and demerits. Gate oxide layer (dielectric) is an essential part of a transistor compare to the graphene channel. Optical visualization of graphene required 300 nm of SiO_2 capping layer over the back gate limits device performance.[3−7] Side-gated graphene FETs does not require any gate dielectric, which degrades the channel mobility. Hahnlein et al. reported high transconductance of G-FETs based on side-gate configuration.[8] At the same time transconductance and current−voltage ($I-V$) characteristics studies of side-gate-FETs are inadequate. As compared to back-gate and side-gate configurations, top-gated graphene FETs (TG-FETs) have the authorized control over the electronic properties of graphene channel,[9] which is due to the freedom of altering the dielectric material and its thickness.

The performance of TG-FET device is mainly dependent on the gate dielectric materials (high dielectric constant (k)) such as HfO_2, Al_2O_3, and ZrO_2.[10,11] Depositing a high-quality gate dielectric without introducing defects on graphene lattice is a challenging task in the transistor fabrication process.[12] Although, atomic-layer deposition (ALD) is the common technique to deposit high-k dielectrics, which requires a initial functionalization process prior to the deposition. This results in the breaking of the chemical bond, defective structure, and even doping of unwanted impurities on graphene lattice, which can significantly affect the device mobility, on/off ratio, conductance, and subthreshold swing, and may also increase the noise level of G-FETs.[12−14] To overcome this performance degradation of graphene device, Liao et al. developed a concept of self-aligned gate electrodes based on $Co_2Si-Al_2O_3$ core−shell nanowire as a gate electrode.[15] The self-aligning method simplifies the lithographic process and minimizes the capacitance overlap. In this letter, we report a new type of G-FET device based on ZnO microwire as a top-gate electrode with self-induced dielectric layer. Surface-adsorbed[16] oxide layer of ZnO act as dielectric layer in this study. The high-k value of ZnO provides enough capacitance to control the active graphene channel.

Figure 1a shows a schematic of the graphene/ZnO micro wire hybrid device. Graphene was prepared from highly oriented pyrolytic graphite (HOPG) by the micromechanical cleavage method and transferred onto SiO_2 (300 nm)/Si substrate and silver (paste) electrodes were made on both sides of graphene. ZnO microwires with diameters of ~5 μm and lengths of 20−150 μm have been chosen and cautiously placed (vertically) over the graphene layer without damaging the crystal lattice. ZnO microwires were synthesized through thermal vapor-phase transport process for detail growth mechanism (see the Supporting Information, Experimental Section). The devices were heated on a hot plate for 150 °C to remove the surface-adsorbed oxygen; silver contacts were made on both sides of the hot microwire. The device was cooled to room temperature to readsorb the oxygen on the remaining parts of the ZnO microwire, making it insulating, and the wire underneath the silver contact remains more conducting than the rest of the wire. A field-emission scanning electron microscopy (FESEM) image of the fabricated self-induced

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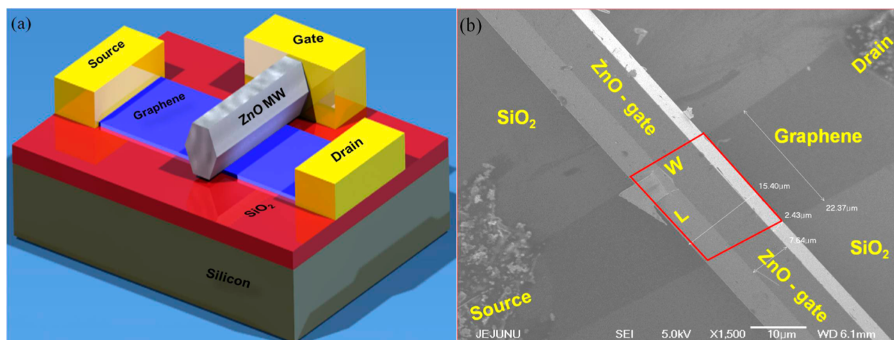

Figure 1. (a) Schematic of graphene FET device with ZnO microwire as a self-induced top-gate electrode, (b) typical FE-SEM image of self-induced top-gated graphene-FET (STG-FET).

top-gated (ZnO microwire) graphene-FET (STG-FET) is shown in Figure 1b. After the fabrication of STG-FETs, Raman spectroscopy measurement was done with 514 nm Ar^+ ion laser as an excitation light source using Horiba Jobin Yvon LabRAM HR800 system. Raman spectrum of ZnO microwire is illustrated in Figure 2a and manifests the material quality and

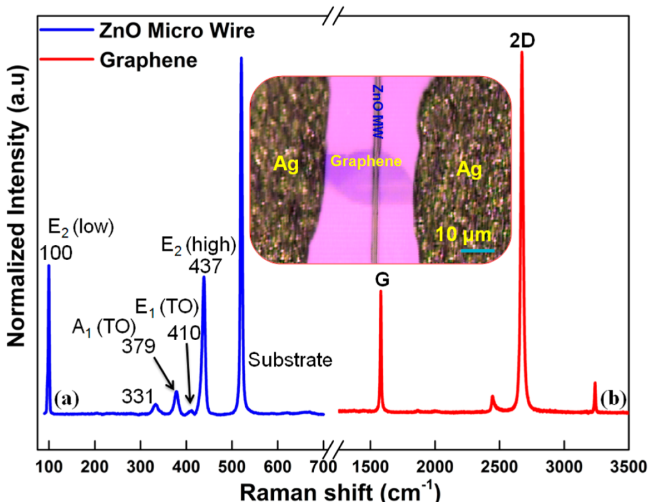

Figure 2. Raman spectrum of (a) ZnO microwire and (b) single-layer graphene. Inset shows the optical microscopy image of a STG-FET device.

wurtzite crystal structure of the synthesized ZnO microwire. Zone center optical phonon modes for the Wurtzite crystal structure of ZnO microwire are A_1+$2B_1$+E_1+$2E_2$.[17] Group theory predicts that the two B_1 modes are Raman inactive and all the other modes are first-order Raman-active. The heavier Zn sublattice with nonpolar vibrations is the reason for the low-frequency E_2 mode. The high-frequency E_2 mode predominantly involves the oxygen atoms. The second-order Raman peak at 331 cm^{-1} is attributed to the acoustic phonons.[18] The two peaks at 379 and 410 cm^{-1} in the spectrum correspond to A_1 (TO) and E_1 (TO) modes, respectively. The peaks corresponding to the LO modes are not present in the obtained spectrum. The peaks at 100 and 437 cm^{-1} are associated with the two nonpolar Raman-active $2E_2$ (low and high) modes.[19] The line width of the E_2 (high) mode is about 7.5 cm^{-1}, whereas the line width of E_2 (low) is about 2.4 cm^{-1}. The corresponding peaks and line width values of the Raman spectrum confirm that the top-gated material is ZnO microwire.

Figure 2b shows the Raman spectrum of single layer graphene. Absence of D peak (defect) reveals the material quality. The full width at half-maximum (fwhm) of 2D peak is ∼22 cm^{-1} and the intensity ratio between 2D and G peaks is 2.9 these values indicates that, the STG-FET device was successfully fabricated on SiO_2/Si substrate without causing any material damage. The inset in Figure 2 is the optical microscopy image of the fabricated STG-FET device. ZnO microwire plays an immense role, which defines the channel length (with respect to the width of the graphene layer), diameter of the microwire sets channel width and also working as a top-gate electrode. The active channel width (W) and length (L) of the STG-FET device is showed in Figure 1b. The surface oxide or depletion layers of ZnO microwire is pretended as gate dielectrics. The electrical characteristics of the device were measured by Agilent, B1500 A semiconductor parameter analyzer.

Gate oxide or depletion layer thickness of the STG-FET can be approximated by[20,21]

$$t = \left(\frac{2\varepsilon_0 \varepsilon_{ZnO} V}{e N_D}\right)^{1/2} \quad (1)$$

Here ε_o is the permittivity of free space, ε_{ZnO} is the dielectric constant of the top-gated ZnO microwire and is ∼8.7,[20] e is electron charge, V is applied potential with order of 1 V, and N_D is the free electron carrier density and is $\sim 1 \times 10^{17}$ cm^{-3}. The thickness of the top-gate dielectric layer is approximated to be 98 nm. The top-gate capacitance (C_{TG}) of STG-FET is estimated to be C_{TG} = 78 nF/cm^2, corresponding to a relative dielectric constant of ∼8.7 with dielectric layer thickness of ∼98 nm for the ZnO microwire.

Electrical transport studies of fabricated STG-FET were carried out in ambient conditions. Self-aligned gate-dependent drain current (I_{ds}) versus drain voltage (V_{ds}) is shown in Figure 3a. The applied top-gate voltage was increased from −30 to 30 V with the step of 10 V. Figure 3a clearly shows that the gate voltage increases toward positive direction the device conductance decreases which is due to the influence of surface adsorbates.[11,22] In ambient conditions, the free charge carriers of ZnO microwire were depleted by the surface adsorbates. Consequently the electronic transport property of top-gated ZnO microwire is dominated by the injected electrons. Absorbance of O_2 from ambient condition form a depletion layer over the ZnO microwire surface with a thickness of ∼98 nm reduces the carrier concentration of ZnO microwire.[20,22]

Top-gate voltage-induced carrier concentration is given by n = $((\varepsilon_o \varepsilon_{ox} V_{TG})/(t_{ox} e))$, where e is electron charge, and V_{GT} is a

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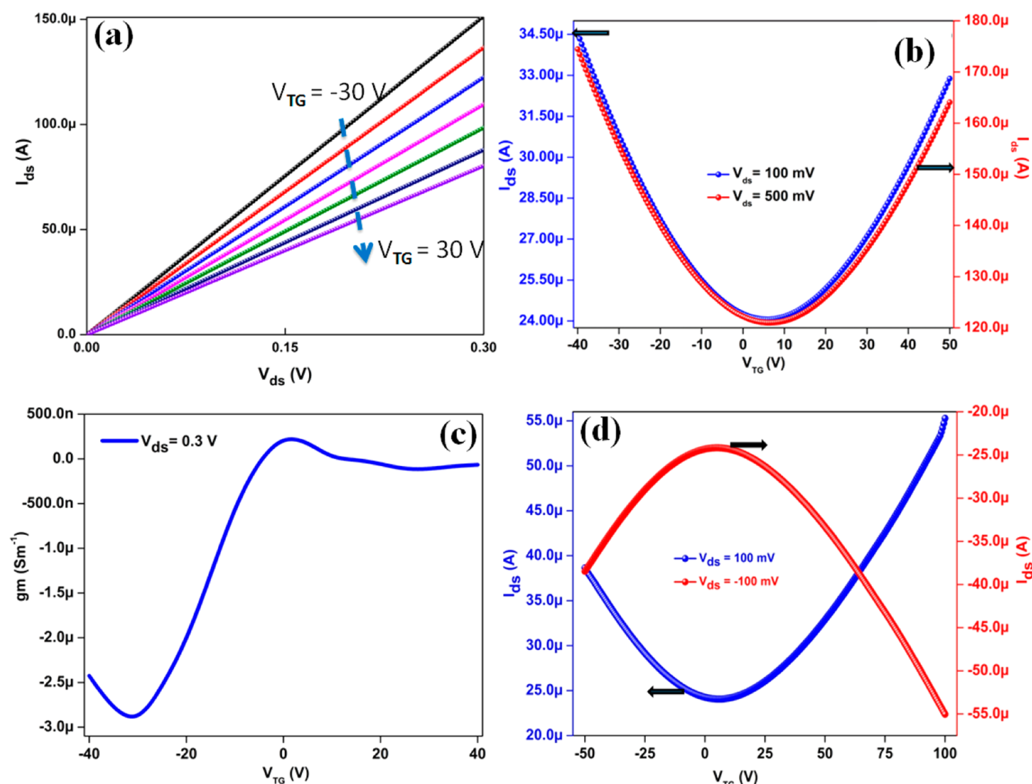

Figure 3. (a) Output characteristic (I_{ds}−V_{ds}) of STG-FET recorded at different gate voltage from −30 to 30 V with the step of 10 V. (b) Transfer characteristics (I_{ds}−V_{TG}) of STG-FET at the drain source voltage of 100 mV, 500 mV during the sweep of top-gate bias from −40 to 50 V. (c) Transconductance (g_m) of STG-FET as a function of top-gate voltage at V_{ds} of 300 mV. (d) Transfer characteristics of STG-FET at two different channel bias voltage.

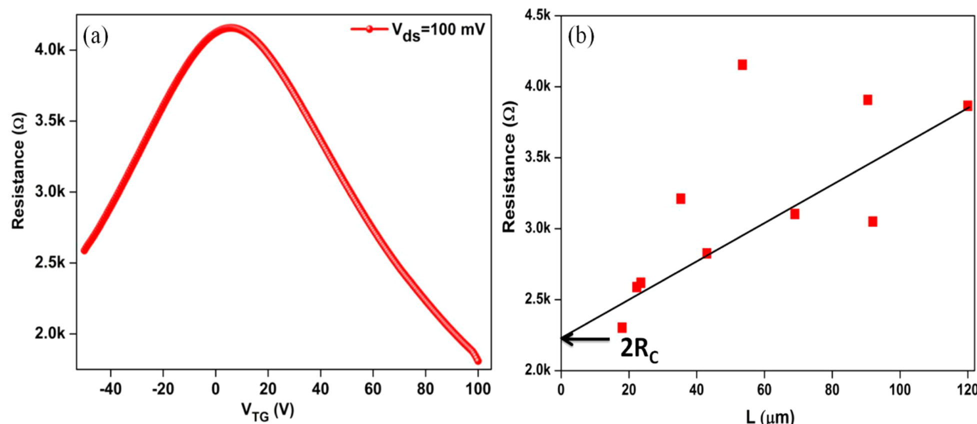

Figure 4. (a) Total resistance (R_T) versus self-induced top-gate voltage (V_{TG}), (b) total resistance versus channel length (R_T−L) plot of STG-FET devices.

top-gate voltage. For typical V_{GT} = 50 V, the formula yields n = 2.45 × 10^{12} cm^{-2} for the STG-FET device. The transfer characteristics of drain−source current (I_{ds}) vs self-induced top-gate voltage (V_{TG}) of the STG-FET device at V_{ds} = 100 and 500 mV is shown in Figure 3b. At V_{TG}= 0 V, the device shows p-channel operation and a perfect symmetric ambipolar behavior was observed with the Dirac point located at 5 V of gate voltage. We observed one order increment in drain current (I_{ds}) with respect to drain voltage (V_{ds}). The STG-FET device can delivers an on-current of 175 μA at V_{ds} = 500 mV for V_{TG} = −40 V and the room temperature on/off current ratio of the device is 55 at V_{ds} = 500 mV.

Figure 3c represents the gate-dependent transconductance of STG-FET, which is defined as g_m = dI_{ds}/dV_{TG} and the transconductance of the device significantly varied with respect to the applied gate potential. The peak transconductance values are found to be 275 nS for positive branch (n-type) and 2.9 μS for negative branch (p-type) of $V_{TG.}$ The hole branch current is larger than electron branch current, which leads to high field effect mobility of 3588 $cm^2/(V\ s)$ for holes and 340 $cm^2/(V\ s)$ for electron (including the contact resistance). The mobility values are derived through transconductance method μ_{DEV} = $((g_mL)/(V_DWC_{TG}))$, here channel length L is 53.5 μm, and channel width W is 5.5 μm. This huge difference in device mobility arises because of the greater number of negative

charges induced on ZnO microwire surface by the positive voltage, which leads to the increment in oxide layer thickness resulting in the reduction of transconductance. Figure 3d shows the transfer characteristics of STG-FET device at different channel bias. At different bias voltage, the device delivers the same amount of current. The minimum conductance is reproduced when applying the negative drain voltage. It suggests that the surface-induced oxide layer does not affect by the channel bias.

Figure 4a shows the resistance (R) as a function of top-gate voltage at V_{ds} = 100 mV. The maximum resistance reveals the charge neutrality point (Dirac point) of the device. To calculate the device mobility value, it is necessary to exclude the contact resistance that is comparable to the device channel resistance. Transfer length measurement (TLM) method has been used to measure contact resistance (R_C) of STG-FET with different channel length. Here the graphene channel width or diameter of the ZnO microwire is ~5 μm. The total resistance (R_T), corresponding channel length (L) (R_T−L plot) of the fabricated device is given in Figure 4b. The contact resistance of STG-FET device was extracted through a linear fit which intercept at L = 0, gives the total contact resistance $2R_C$ = 2.2 KΩ. The total resistance of the STG-FET device can be expressed with the following relation[23,24]

$$R_{total} = 2R_C + R_{channel} = 2R_C + \frac{L}{We\mu\sqrt{(n_0^2 + n^2)}} \quad (2)$$

where R_{total} is the total resistance of the STG-FET device. R_C is the metal/graphene contact resistance. $R_{channel}$ is the resistance of the graphene channel covered by self-induced top-gate electrode, e is electron charge, μ is the mobility of the device, n is the carrier concentration induced in graphene channel by top-gate electrode, and n_0 is the residual carrier concentration of graphene, which is generated by charged impurities[25] present in the graphene/ZnO microwire interface (n_0 = 2.45 × 10^{11} cm^{-2} for STG-FET device). The channel length is L and the width of the channel is W.

The extracted STG-FET device mobility (μ) based on the diffusive transport model state in eq 2 is exceeds 1630 $cm^2/(V\ s)$ for holes and 1240 $cm^2/(V\ s)$ for electrons. This present study shows that the ZnO microwire can be used as a top-gate electrode for G-FETs device without depositing any dielectric layer.

In summary, we have fabricated a graphene-FET device with ZnO microwire as a top-gate electrode. The depletion layer of the ZnO microwire is act as a gate dielectric for G-FETs with thickness of ~98 nm. The device characteristics are well agreed with the existing device models. The STG-FET device gives an on-current of 175 μA, on/off current ratio of 55, and device mobility exceeding 1630 $cm^2/(V\ s)$ for holes and 1240 $cm^2/(V\ s)$ for electrons at room temperature. Self-induced gate dielectric process prevents the G-FETs from impurity doping, defect formation in graphene lattice and facilitates the fabrication process. The performance degradation of G-FETs can be overcome by our device structure.

■ ASSOCIATED CONTENT

Ⓢ Supporting Information

The detailed synthesis process of ZnO microwire used for the fabrication of G-FET device is given along with a schematic diagram. This material is available free of charge via the Internet at http://pubs.acs.org/.

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Notes

The authors declare no competing financial interest.

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